WHAT IS CLAIMED IS:

1. A data processor for demodulating a series of data including the predetermined mark for detecting synchronization, comprising:

receiving unit for receiving the series of data in a plurality of parallel bits; and

detecting unit for detecting said predetermined mark for detecting synchronization from the parallel data.

2. A data processor according to claim 1, wherein said detecting unit detects the predetermined mark for detecting synchronization in a predetermined bit width among the series of data in the parallel condition.

3. A data processor according to claim 1, further comprising a generation timing selecting unit for selecting the generation timing of the window for detecting predetermined mark based on the predetermined mark for detecting synchronization.

4. A data processor according to claim 1, further comprising a data demodulating unit for demodulating the series of data between the predetermined marks for detecting synchronization based on the predetermined mark for detecting synchronization.

5. A data processor according to claim 1, further comprising a detection line memory unit for storing the detection line based on the predetermined mark for detecting synchronization.

6. A data processor according to claim 1, further comprising a data selecting unit for selecting the data based on the predetermined mark for detecting synchronization.

7. A data processor according to claim 1, further comprising a data counting unit for counting the series of data between the predetermined mark for detecting synchronization based on the predetermined marks for detecting synchronization.

8. A data processor according to claim 1, further comprising

a data selecting unit for selecting the data based on the predetermined mark for detecting synchronization.

9. A data processor according to claim 1, wherein said receiving unit is provided with a shift register to input the data of a plurality of parallel bits connected with the detecting unit in the same number as the number of parallel bits.

10. A data processor for detecting the predetermined mark for detecting synchronization included in a series of data read from the memory medium in order to establish the synchronization at the time of transferring the series of data to the controller unit from the read channel unit and for demodulating the series of data between the predetermined marks for detecting synchronization, comprising:

a receiving unit for receiving the series of data in a plurality of parallel bits; and

a detecting unit for detecting the predetermined mark for detecting synchronization from the parallel data.

11. A data processing method for demodulating a series of data including the predetermined mark for detecting synchronization, comprising the following steps of:

receiving the series of data in a plurality of parallel bits;

detecting the predetermined mark for detecting synchronization from the parallel data to establish the synchronization of the series of data; and

demodulating the data based on the predetermined mark for detecting synchronization included in the series of data.

12. A data processing method according to claim 11, wherein the predetermined mark for detecting synchronization are detected in a predetermined bit width of the series of data in the parallel condition.

13. A data processing method according to claim 11, wherein the generation timing of the window for detecting predetermined mark is

selected based on said detected predetermined mark for detecting synchronization.

14. A data processing method according to claim 11, wherein the detection line is stored based on the detected predetermined mark for detecting synchronization.

15. A data processing method according to claim 11, wherein data is selected based on the detected predetermined mark for detecting synchronization.

16. A data processing method according to claim 11, wherein data between the detected predetermined marks for detecting synchronization is counted up.